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(71) Applicant (*for all designated States except US*): NATIONAL UNIVERSITY OF SINGAPORE [SG/SG]; 10 Kent Ridge Crescent, Singapore 119260 (SG).

(72) Inventors; and
(75) Inventors/Applicants (*for US only*): LIANG, Yung, Chii [SG/SG]; 113 Clementi Street 13 #03-27, Singapore 120113 (SG). SAMUDRA, Ganesh, Shankar [IN/SG]; 111 Clementi Road, Block C, #08-03, Singapore 129792 (SG). GAN, Kian, Paau [MY/SG]; 35 West Coast Park, #04-03, Singapore 127652 (SG). YANG, Xin [CN/SG]; 18A West Coast Road, Greenacres #01-03, Singapore 127307 (SG).

(74) Agent: ALBAN TAY MAHTANI & DE SILVA; 39 Robinson Road #07-01, Robinson Point, Singapore 068911 (SG).

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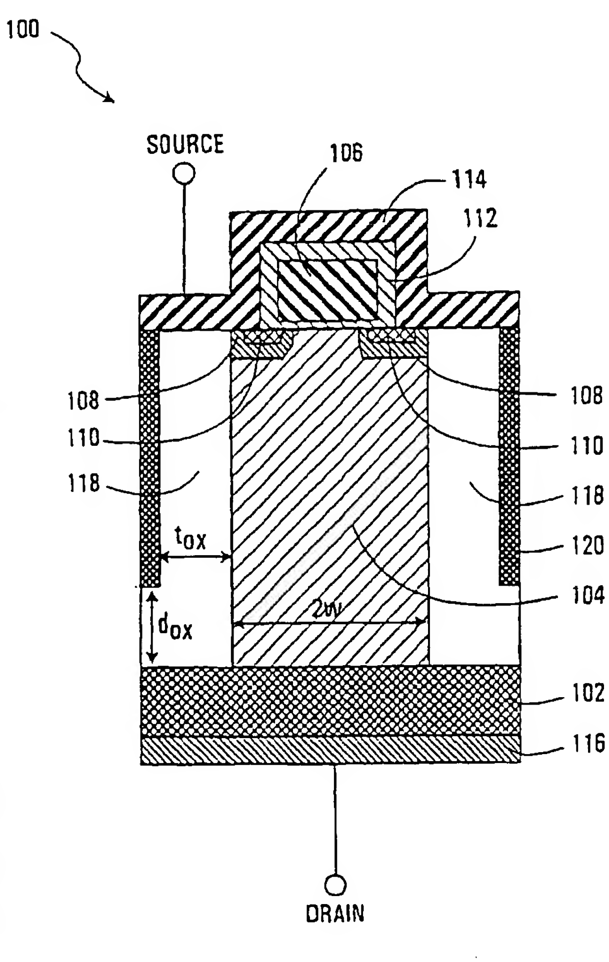

(57) Abstract: A MOSFET (100) includes a dielectric, preferably in the form of a metal thick oxide (118) that extends alongside the MOSFET's drift region (104). A voltage across this dielectric between its opposing sides exerts an electric field into the drift region to modulate the drift region electric field distribution so as to increase the breakdown voltage of a reverse biased semiconductor junction between the drift region and body region (108). The voltage is applied to conductive region (120). This allows for higher doping of the drift region, for a given breakdown voltage when compared to conventional MOSFET's. The MOSFET is made by forming opposed vertical trenches in a semiconductor wafer, covering the walls of the trenches with dielectric (118), filling the trenches between the dielectric with conductive material (120), and forming a double diffused MOSFET structure between the pair of opposed vertical trenches such that a drift region abuts the dielectric material (118).

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POWER MOSFET HAVING ENHANCED BREAKDOWN VOLTAGE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims benefits from U.S. Provisional Patent Application No. **60/295,581** filed June 5, 2001, the contents of which are hereby incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates generally to power semiconductor devices, and more particularly to metal oxide semiconductor field effect transistors (MOSFETs) for high voltage and high current applications.

BACKGROUND OF THE INVENTION

In power electronics applications MOSFETs have become the devices of choice for switching high voltages and currents. When compared to bipolar devices, they have fast switching times and simple gate drive circuitry. Specifically, the double-diffusion MOSFET structure is favoured as it allows easy fabrication and self-alignment of channel length control. In such a MOSFET, current flows between transistor drain and source through a lightly doped drift region and a conduction channel that is electrically formed in the body of the transistor.

Current conduction between drain and source is electrically controlled by a voltage applied to a gate that exerts an electric field on the transistor body to form the channel. The magnitude of the gate voltage varies the channel depth and its conductivity. Application of a gate voltage may

thus be used to switch the transistor between its on and off states. In its on state, the resistance from source to drain includes the resistance of the transistor's drift region. In fact, for most power MOSFETs, the drift region resistance is the dominant component of overall on-state resistance, as MOSFETs are majority carrier devices and only limited excess carriers are injected into the drift region to modulate its resistance in the MOSFET's on-state. Of course, high conductivity (and therefore low resistance) of this drift region for high current conduction is extremely desirable. Due to absence of effective modulation mechanism affecting resistance, conductivity of the drift region is mainly dependent on, and proportional to, the background doping concentration of this region.

In the MOSFET's off-state, the body region to drift region junction prevents conduction of current, provided that the potential difference across this junction does not exceed the avalanche or punch-through breakdown voltage of the junction. Almost the entire potential drop is in the drift region at drain side of this junction. The potential drop across the body region and the source region is significantly smaller than that of the drift region due to the much higher doping concentration of the body and source regions. The electric field profile in the drift region has its maximum amplitude at the junction and decreases linearly when moving away from the junction, eventually to zero. How quickly the field drops when moving away from the junction is strongly influenced by the drift region's background doping concentration. The total integrated area under the field distribution is equal to the voltage across the junction. A higher doping concentration will make the field drop more quickly, creating a higher peak junction field for the same amount of the voltage applied compared to a lower doping region.

Thus a higher doping in the drift region not only makes the on-state resistance lower but also decreases the off-state breakdown voltage of the body region to drift region junction. In conventional double diffused silicon MOSFETs, there exists a trade-off limit between the specific on-

state resistance, $R_{on,sp}$ and the off-state breakdown voltage, BV_{dss}, i.e. $R_{on,\ sp} \propto BV_{dss}^{2.5}$, as for example described in C. Hu, "Optimum doping profile for minimum ohmic resistance and high breakdown voltage", *IEEE Transactions on Electron Devices*, Vol. ED-26(3), pp. 243-245, 1979. As such, power MOSFET designers are constantly seeking ways to lower drift region resistance without reducing the body region to drift region junction breakdown voltage.

Recently, proposed MOSFET designs alternately stack p and n layers to overcome the silicon trade-off limit, as for example illustrated in U.S. Patent Nos. 5216275, 5438215 and European Patent EP0053854. These disclosed devices all rely on the charge compensation principle of the alternating p and n layers to increase the permissible doping of the device so that the relationship between on-state resistance and off-state breakdown voltage can be improved.

Another approach disclosed in U.S. Patent No. 5637898 proposes a linearly graded doping profile to modulate the field distribution in the drift region. The width of the drift region is limited as the linear profile is achieved by the angled implantation from trenched sidewalls.

All of these proposed MOSFETS are, however, difficult to fabricate, involving expensive multi-epitaxy process, as for example detailed in G. Deboy, M. Marz, J.-P. Stengl, H. Strack, J. Tihanyi and H. Weber, "A new generation of high voltage MOSFETs breaks the limit line of silicon", *IEEE IEDM Technical Digest*, pp. 683-685, 1998.

Subsequent developments have been aimed at achieving the charge compensation by other processes as for example detailed in T. Nitta, T. Minato, M. Yano, A. Uenisi, M. Harada and S. Hine, "Experimental Results and Simulation Analysis of 250V Super trench Power MOSFET (STM)", *Proc. 12th Int. Symp. Power Semiconductor Device and ICs*, pp. 77-80, 2000, T. Minato, T. Nitta, A. Uenisi, M. Yano, M. Harada and S.

Hine, "Which is cooler, trench or Multi-Epitaxy?", *Proc. 12th International Symposium on Power Semiconductor Device and ICs*, pp. 73-76, 2000, and in J. Glenn and J. Siekkinen, "A VDMOS vertical deep trench RESURF DMOS (VTR-DMOS)", *Procedure 12th International Symposium on Power Semiconductor Device and ICs*, pp. 197-200, 2000. These newer processes are generally limited by the narrow window imposed by the precise charge balance needed to achieve the optimum on-resistance and the p/n layer inter-diffusion, as for example explained in P. M. Shenoy, A. Bhalla and G. M. Dolny, "Analysis of the effect of charge imbalance on the static and dynamic characteristics of the super junction MOSFET", *Proc. 11th International Symposium on Power Semiconductor Device and ICs*, pp. 99-102, 1999.

Accordingly, there is need for an improved power MOSFET, having an improved breakdown voltage to on-state resistance relationship.

SUMMARY OF THE INVENTION

The present invention proposes a new approach to increasing MOSFET breakdown voltage, which is easier to realise and thus yields a better control than existing MOSFET designs. In accordance with an aspect of the present invention, a MOSFET includes a dielectric, preferably in the form of a metal thick oxide, that extends alongside the MOSFET's drift region. A voltage across this dielectric between its opposing sides exerts an electric field into the drift region to increase the breakdown voltage of a reverse biased semiconductor junction between the drift region and body region. This allows for higher doping of the drift region, for a given breakdown voltage when compared to conventional MOSFETs.

In accordance with a first aspect of the present invention, a power MOSFET includes a source region; a drain region; a gate; a body region; and a drift region extending between the body region and drain region, to

at least partially guide current from the drain region to the source region and a dielectric having opposing sides. One of these opposing sides extending alongside the drift region, and an opposite one of its opposing sides connected to a conducting region, so that a voltage across the dielectric between its opposing sides exerts an electric field into the drift region to redistribute free carriers in the drift region and thereby affect the electrical field distribution in the drift region to increase the breakdown voltage of a reverse biased semiconductor junction between the drift region and the body region.

In accordance with another aspect of the invention, a method of forming a metal oxide semiconductor transistor (MOSFET) in a semiconductor wafer includes, forming opposed vertically extending trenches in the semiconductor wafer; covering interior walls of each of the trenches with a dielectric material of a defined thickness; filling a volume of each of the trenches between the dielectric material with a conductive material; forming a double diffused MOSFET structure between the opposed vertical trenches, the MOSFET structure formed to have a drift region that abuts the dielectric material along at least a portion of its vertical extent.

Conveniently, this allows a lower specific on-state resistance, $R_{on,\ sp}$ at a given drain to source voltage BV_{dss} than dictated by the conventional limit, without using expensive and complicated process technology.

Precise charge compensation is not required. Instead it is the oxide thickness that is controlled for optimal performance.

Other aspects and features of the present invention will become apparent to those of ordinary skill in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

In the figures which illustrate by way of example only, embodiments of the present invention,

FIG. 1 illustrates a conventional planar gate MOSFET;

FIG. 2A illustrates a planar gate MOSFET, exemplary of an embodiment of the present invention;

FIG. 2B illustrates an electric field distribution for the MOSFETs of **FIGS. 1** and **2A**;

FIG. 3 illustrates a trench gate MOSFET, exemplary of another embodiment of the present invention;

FIGS. 4, 5A-5B, 6A-6B, 7, 8 and **8A-8C** illustrate exemplary stages in processes of forming a MOSFET exemplary of an embodiment of the present invention on a semiconductor wafer;

FIG. 9 illustrates the relationship of specific on-state resistance as a function of breakdown voltage for the MOSFET of **FIG.2A**;

FIG. 10 illustrates the relationship between breakdown voltage and dielectric column width for the MOSFET of **FIG. 2A**;

FIG. 11 illustrates a section of p-i-n structure used to approximate performance of the MOSFETs of **FIG. 2A** and **FIG. 3**;

FIG. 12 illustrates measured reverse bias currents of equivalent p-i-n structures for conventional MOSFETs and the MOSFET of **FIG. 2A**;

FIG. 13 illustrates a further trench gate MOSFET, exemplary of another embodiment of the present invention;

FIG. 14 illustrates the relationship between breakdown voltage and control voltage for the MOSFET of **FIG. 13**;

FIG. 15 illustrates specific on-state resistance to breakdown voltage for the MOSFET of **FIG. 13**; and

FIGS. 16 and **17** illustrate the relationship of small-signal transconductance gains and bandwidth to gate voltage for the MOSFETs of **FIGS. 2A** and **13**.

DETAILED DESCRIPTION

FIG. 1 illustrates a conventional planar gate, n-channel power MOSFET **10**. MOSFET **10** is formed on a heavily doped n+ semiconductor substrate **12**. A more lightly doped epitaxial layer, defining a drift region **14**, is grown on substrate **12**. At the top of the epitaxial layer, p type body regions **18** are formed. n+ source regions **20** are formed within body regions **18**. A gate **16** is formed atop region **14** and overlaps p-type body regions **18**. Gate **16** is insulated from drift region **14** and p-type body regions **18** by an oxide layer **22**. Gate **16** is preferably formed from a heavily doped poly-silicon. Metal contacts **24** and **26** are formed for electrical interconnection of source regions **20** and substrate **12** to allow these to act as source and drain contacts, respectively.

As is understood, current may flow between drain and source in the presence of an n channel between the source region and n drift region **14**. An applied voltage at gate **16** exerts a field creating a thin inversion mobile charge zone underneath the gate oxide layer **22** in p-type body regions **18**, defining the conducting n channel from source region **20** into drift region **14**. The resistance from source contact **24** to drain contact **26** is in large part attributable to the resistance of the drift region **14**. The resistance of the drift region **14**, in turn, is inversely proportional to the

available free carriers and therefore the concentration of dopants N_d in the drift region **14**.

In the absence of a voltage at gate **16** MOSFET **10** is in its off-state, and the p-n junction between the p body region **18** and the n drift region **14** is reverse biased. Below a breakdown voltage this junction sustains the drain to source voltage and, except for a small leakage current, prevents the flow of current from drain to source. As will be appreciated, breakdown of this junction occurs if the electric field at the junction exceeds a defined avalanche value, E_0. For silicon $E_0 = 8 \times 10^5$ V/cm, at room temperature.

For the described pn junction, the breakdown voltage, V_{br} may be expressed in terms of the electric field avalanche value, E_0, and n doping, N_d as

$$V_{br}^{4/3} = (\varepsilon_{si} E_0^2) / (2 q N_d) \qquad (1)$$

where ε_{si} is the dielectric constant of the silicon material and q is the electron charge. Clearly, while conductivity is proportional to the background doping of the drift region **14**, the breakdown voltage of the body region to drift region junction is inversely proportional to the same doping level.

FIG. 2A illustrates a MOSFET **100**, exemplary of an embodiment of the present invention. Like a conventional MOSFET **10** (**FIG. 1**) MOSFET **100** is formed on a heavily doped n+ semiconductor substrate **102**. A more lightly doped epitaxial layer defining drift region **104** is grown on substrate **102**. At the top of region **104**, p-type body regions **108** are formed. n+ source regions **110** are formed within body regions **108**. A gate **106** is formed atop the epitaxial layer across the p-body regions to reach source regions **110**, and is insulated therefrom by an oxide layer **112**. Metal contacts **114** and **116** are formed for electrical interconnection source regions **110** and substrate **102** to act as source and drain

contacts, respectively.

Additionally, MOSFET **100** includes sidewall metal-thick-oxide (MTO) dielectric columns **118**. Each of dielectric columns **118** extends vertically at the opposite edges of n drift region **104**. As such, drift region **104** resembles a column having width 2w. One edge of each dielectric column **118** is adjacent to n drift region **104** of MOSFET **100**. The opposite edge of each column **118** is bounded by a vertically extending conductive region **120**. Preferably each conductive region **120** is formed of a p+/n+ poly-silicon semiconductor. As well, conductive regions **120** are electrically connected to source metal contact **114**.

FIG. 2B illustrates the electric field distribution as a function of distance from the body region to drift region junction for MOSFET **100** and MOSFET **10** in their off-state. Functionally, for MOSFET **100** in its off-state, the voltage across each column **118** deposits a charge at the edge of each column **118**. This charge, in turn, exerts an electric field on drift region **104** that depletes free carriers in the n column of the drift region **104** laterally. That is, free carriers are redistributed within drift region **104**. This alters the original vertical field distribution within the drift region **104** to have a shape as illustrated in **FIG. 2B.** That is, the vertical field magnitude is no longer a linear triangle-like distribution like that in MOSFET **10**, but a square-like distribution as shown. As noted, the voltage across the junction equals the integral of the field distribution. As such, for the same voltage the peak magnitude of the field across the junction of MOSFET **100** will be less than the peak magnitude of the field across the junction of MOSFET **10**.

Preferably, the sidewall oxide is thermally grown to obtain the highest breakdown quality, or if any other dielectric material is chosen to replace the oxide, it should have a breakdown field strength equal to or greater than that of the thermal oxide. The dielectric thickness needs to be properly controlled as described below.

Quantitatively, the voltage drop across column **118** (i.e. the lateral voltage drop) can be approximated as,

$$V \approx (Q\, t_{ox}) / (\varepsilon_{ox} A) = (q\, N_d\, w\, t_{ox}) / \varepsilon_{ox} \qquad (2)$$

where, Q is the charge at the surface of the column **118**, t_{ox} is the oxide thickness, ε_{ox} is the oxide dielectric constant, A is the sidewall area, and q is the electron charge. Q at the surface of column **118**, in turn, depletes free carriers from the n drift region **104**.

Ideally, in order to have an optimal effect on the breakdown voltage in the body, the charge at the surface of column **118** should deplete the entire n-drift region just before breakdown, thus solving equations (**1**) and (**2**), yields

$$N_d \approx [\,(\varepsilon_{si} \,.\, E_0^{2} \,.\, \varepsilon_{ox}^{4/3}) / (\,\mathbf{2} \,.\, q^{7/3})\,]^{3/7} \,.\, [\,t_{ox} \,.\, w\,]^{-4/7}$$

$$= \mathbf{2.90 \times 10^{11}} \,.\, [\,t_{ox} \,.\, w\,]^{-4/7} \qquad (3)$$

Equation (**3**) defines the mathematical relationship among doping concentration of the drift region **104**, the sidewall oxide thickness of column **118** and the half width (w) of the drift region **104** to function at its preferred breakdown voltage.

MOSFET **100** will have a desired optimal breakdown voltage for a particular N_d as long as any combination of the three design parameters, N_d, t_{ox} and w satisfy equation (3).

The specific on-state resistance between drain and source $R_{on,sp}$ is calculated to be proportion to $(w + w_{MTO}) / (N_d \times w)$ where the trench column half-width, w_{MTO} is the sum of sidewall oxide thickness and the electrode half-width, w_{elec}, that is, $w_{MTO} = t_{ox} + w_{elec}$. It may be shown that an optimal ratio of w_{MTO} to w of **4**:**3** exists for minimum $R_{on,sp}$. The thickness of the bottom oxide d_{ox} can be chosen to be the same as or preferably greater than t_{ox}.

Owing to this additional field modulation by lateral depletion, the doping in the drift region **104** can be raised to a value much higher than that permissible in conventional MOSFETs such as MOSFET **10**, thus improving the specific on-resistance to breakdown voltage relationship curve for silicon MOSFET **100**. In contrast to known ways of increasing breakdown voltage as for example, suggested in noted US patent Nos. 5216275, and 5438215, no precise matching of doping is needed in MOSFET **100**. Instead, for a particular drift region width **2**w and doping N_d (as shown in **FIG. 2A**), it is primarily the sidewall thickness of each column **118**, t_{ox}, that needs to be controlled to provide the optimal field effect to deplete the column of the n drift region **104** entirely during the off-state.

Conveniently, as oxide thickness control technology is well-known, MOSFET **100** can be easily and precisely manufactured than known charge compensation structures that require the difficult task of precise doping control and multiple epitaxial growth.

As will be appreciated, MOSFETs exemplary of the present invention may be either planar gate MOSFETs (like MOSFET **100** illustrated in **FIG. 2A**), or trench gate MOSFETs (like MOSFET **140** illustrated in **FIG. 3**). Elements of MOSFET **140** are akin to those of MOSFET **100** (**FIG. 2**) and are therefore labelled with like numerals bearing a double prime (") symbol in **FIG. 3**.

As illustrated in **FIG. 4**, an epi wafer **150** with suitable Si (100) n-epi thickness and doping N_d is used as starting wafer. Suitable masking materials, for example oxide and nitride layers **152**, **154** respectively, are first deposited.

Thereafter, vertically extending trenches **160** to accommodate columns **118** (**FIG. 2A**) of suitable dimensions are etched on the wafer **150**, as illustrated in **FIG. 5A**. Preferably, trenches **160** are laterally mirrored.

The region between trenches **160** defines drift region **104**. If the starting wafer is constrained to have different background doping, as for example required by some smart power ICs, then an optional tilted implantation may be performed, as illustrated in **FIG. 5B** to adjust the background doping in the n drift region column, as required.

Next, a suitable wet oxidation step giving the required thickness t_{ox} of column **118** is performed and all the masking materials are then stripped, as illustrated in **FIG. 6A**. This covers the interior sidewalls and floors of trenches **160** with a thick dielectric, like the suggested oxide. Alternatively, if direct wet oxidation cannot get the required dielectric thickness, multiple thin trenches **162** and the subsequent silicon column consumption, as illustrated in **FIG. 6B** may be employed to obtain a thicker side-wall thickness

Highly doped n+ or p+ poly-silicon deposition (for example $POCl_3$ doping) is used to fill up the remainder of trenches **160** as illustrated in **FIG. 7**. This poly-silicon provides the contact region **120** to source metal for columns **118**. The poly-silicon etch-back step is performed to remove any excess poly-silicon on the top surface. Thereafter, the conventional power MOSFET is formed between the trenches using conventional process steps, giving the final MOSFET device structure as shown in **FIG. 2A** (planar gate) or **FIG. 3** (trench gate).

Conveniently, each trench **160** may accommodate two columns **118**, each of which may form part of one of two adjacent transistors formed on wafer **150**.

Optionally, in order to reduce the n drift region **104** column width for larger N_d, the body contact p+ region, usually located laterally next to the n+ source region, can be moved vertically (i.e. upward but still next to the n+ source region). The resulting segmented source will have a smaller width. The layout view for this segmented source design is shown in

FIGS. 8, 8A-8C. Note that both planar and trench gate structures can use this segmented source design to reduce the width of drift region 104.

The principles of operation of MOSFETs 100 and 140 (FIGS. 2A and 3) as conjectured above, have been verified by both simulation and experiment. As noted, MOSFETs 100 and 140 will have an improved breakdown voltage for a given doping of drift region, as long as any combination of the three design parameters, N_d, t_{ox} and w satisfy equation (3). Numerical analysis confirms the existence of an optimal ratio of column 118 half dielectric trench column width to w of 4:3 for lowest $R_{on,sp}$.

By following the above conditions, numerical simulations were carried out and the simulation results illustrated in FIG. 9 show that exemplary MOSFETs 100, 140 have improved the specific on-resistance, $R_{on,sp}$ to breakdown voltage, BV_{dss} trade-off curve compared to the conventional case. In fact, the trade-off curve of MOSFETs 100, 140 was found to have a similar dependence as that of the ideal silicon limit but with a smaller coefficient, to yield a lower on-state resistance. This is in contrast to the charge compensation structures, disclosed in U.S. Patents 5216275 and 5438215, where $R_{on,sp}$ varies at different dependences with BV_{dss} with its coefficient dependent on w, the half width of p and n columns. At present, owing to technology constraints and inter-diffusion problems, the width of the drift region in known charge compensation structures cannot be scaled arbitrarily small, especially at high breakdown voltage where a thick epi (for example 50 μm for 600 V) is needed. Thus at present, a practical value of w would be around 10 μm and at this value, MOSFET 100 (or MOSFET 140) has an off-state performance comparable to charge compensation (superjunction) structure at around 500 V device rating. An even better performance can be obtained for voltage rating below 400 V. Note that, the superjunction structure performs worse than the conventional silicon limit at voltage rating below 280 V.

As previously noted, column **118** sidewall oxide thickness t_{ox} influences performance of MOSFETs **100, 140**. Sensitivity analysis of t_{ox} to BV_{dss} at a nominal value of 1 μm has been performed and the results shown in **FIG. 10**. As illustrated, BV_{dss} in excess of **200** V was achievable with a t_{ox} tolerance of over ±**10** % for designs with $d_{ox} > t_{ox}$. Note that a process simplification, resulting in only a minor degraded breakdown performance, can be made by adopting a $d_{ox} = t_{ox}$ design that can be realised in just a single wet oxidation step.

Since a MOSFET, like MOSFETs **100, 140**, in its off-state is essentially a p-i-n structure, a p-i-n structure with $t_{ox} = d_{ox} =$ **1** μm, w = **2** μm has been fabricated to verify MOSFETs **100, 140** experimentally. The p-i-n structure was fabricated on a $\mathbf{N_d}$ = **7** x **10**^{15} cm^{-3} n-epi starting wafer by following the process flow as detailed above, together with the conventional p-i-n structure without the oxide on the same wafer. Both devices have identical area. Trenches of **4** μm width and **15** μm depth were first etched on the wafer. This was followed by **1** μm wet oxidation step giving a $d_{ox} = t_{ox} =$ **1** μm design. Next, polysilicon deposition with $POCl_3$ doping was used to fill up the trenches. After the poly etch-back step, conventional p-i-n diode process steps proceed as usual giving the final device structure as shown in the scanning electron microscopy picture of **FIG. 11**. It is noteworthy that only one additional mask was needed to complete the whole process compared to conventional case.

FIG. 12 shows a comparison of the measured off-state results of both MOSFETs **100, 140** (as equated by the p-i-n with dielectric oxide column of **FIG. 11**) and conventional devices. It is clear that the measured breakdown voltage of **170** V for MOSFETs **100, 140** as simulated was more than twice that of conventional device at 67 V. Actually, to achieve **170** V a doping of **2** x **10**^{15} cm^{-3} would be required for conventional MOSFETs whereas a doping of **7** x **10**^{15} cm^{-3} may be sufficient for MOSFETs **100, 140**. A $R_{on,\,sp}$ reduction of about twice is thus predicted for MOSFET **100** with similar voltage rating after taking into account the

reduction in conduction area due to the sidewall oxide. Further improvement in $R_{on,\ sp}$ is expected if the area occupied by dielectric column in **FIG. 11** can be reduced without reducing oxide thickness, by using high aspect ratio trench techniques.

FIG. 13 illustrates another MOSFET **200**, exemplary of a further embodiment of the present invention. As illustrated, MOSFET **200** is a trench gate MOSFET. Components akin to those of MOSFETs **100** and **140** are therefore identified with numerals used to describe MOSFETs **100** and **140**, but bearing a prime (') symbol, and are not again explicitly described. In MOSFET **200**, however, source contact **114**' is not electrically connected with column **118**' or conductive region **120'**. Instead, conductive region **120**' is electrically interconnected to its own contact **122** formed atop conductive region **120'**. No contact is interconnected with column **118**'. As a result the voltage drop across column **118**' may be independently controlled through application of a control voltage to contact **122**. Control of the voltage across column **118'**, in turn, controls the charge and the lateral field at the interface between column **118**' and drift region **104**'. Blocking voltage may, in turn, be fine-tuned if the voltage falls short of the specification due to process variations after manufacture through application of an appropriate control voltage to contact **122**.

FIG. 14, in turn, illustrates the predicted breakdown voltage of example MOSFET **200**, determined by numerical simulation, as a function of applied tuning voltage for an example device having N_d=**3**x**10**^{15} cm^{-3}; tox=**1.5** µm and w=**1**.**5** µm.

At the same time, performance of MOSFET **200** in its on-state may be better than that of MOSFET **140**. Specifically, in its on-state, a vertical accumulation layer is formed at the interface between column **118**' and N- drift region due to the lateral electric field produced by the positive bias from conductive region **120'**. This accumulation layer provides additional

path for the current flow in drift region **104'**, and results in the reduction of on-resistance.

FIG. 15 illustrates the relationship between BV_{dss} and specific on-resistance ($R_{on,sp}$) of MOSFETs, like example MOSFET **200**, at different Nd doping values under different control bias voltages at contact **122**, as predicted by numerical simulations. As illustrated, as the control bias voltage is incremented in 10 V increments, from **0**V for each example MOSFET, the breakdown voltage and on-state resistance varies. BV_{dss} can be increased by about **48** V and $R_{on,sp}$ can be reduced by about **1.5** mΩ-cm^2. As illustrated, the minimum $R_{on,sp}$ obtained under **20**V side-poly bias at N_d = $\mathbf{6{\times}10^{15}}$ cm^{-3} is much lower than ideal silicon limit and superjunction devices at a much higher BV_{dss}. It also goes further away from ideal silicon limit line compared to the original MOSFETs **100**, **140** of **FIGS. 2A** and **3**.

As well, in the saturation region of operation, small signal transconductance gain of a MOSFET like MOSFET **200** is determined by the channel and gate structure and bias. When MOSFET **200** is under a positive control bias, the lateral electric field produced by the external bias acts on the channel and pulls the electrons towards the column **118'**. As a result, the inversion layer depth is increased reducing the channel resistance, and the electric field perpendicular to the gate oxide within the channel is diminished giving enhanced channel mobility. This leads to a higher and wider G_m curve.

According to the equation: $F_T=G_m/(2\pi C_{iss})$, where C_{iss} is the sum of gate-source and gate-drain Miller capacitance, the bandwidth F_T will increase correspondingly with the increase of G_m if there is no distinct change in C_{iss}. Simulation results show that the improvement of F_T has the same trends as that of G_m.

FIGS. 16 and **17** illustrate G_m vs. V(Gate) curve and F_T vs. V(Gate) curve

of MOSFETs **100**, **140** with $N_d = 7\times10^{15}cm^{-3}$ and MOSFET **200** for various control voltages, with $N_d = 5\times10^{15}\ cm^{-3}$, at given V_{ds}=30V and small signal source frequency of 1MHz. As illustrated, both families of curves show a larger operational range of the gate voltage under higher control bias.

Of course, the above described embodiments, are intended to be illustrative only and in no way limiting. The described embodiments of carrying out the invention, are susceptible to many modifications of form, arrangement of parts, details and order of performance.

The invention may, for example, be used in both vertically arranged MOSFET structures as described or similar, and in lateral structures where drain and source layers are both located on top of the wafer surface. For application in lateral structures, the dielectric column may be placed in lateral orientation to be along the lateral drift region. Regardless of the orientation of the dielectric, the functional principles on sidewall field exertion and modulation of the breakdown field in the drift region remain the same.

The proposed invention can be applied to power MOSFETs made of materials other than silicon. It may also be used in p-channel MOSFETs.

The invention, rather, is intended to encompass all such modification within its scope, as defined by the claims.

WHAT IS CLAIMED IS:

1. A power metal oxide semiconductor field effect transistor (MOSFET), comprising:

a source region;

a drain region;

a gate;

a body region;

a drift region extending between said body region and drain region, to at least partially guide current from said drain region to said source region;

a dielectric having opposing sides, one of its opposing sides extending alongside said drift region, and an opposite one of its opposing sides connected to a conducting region, so that a voltage across said dielectric between its opposing sides exerts an electric field into said drift region to redistribute free carriers in said drift region and thereby affect the electrical field distribution in said drift region to increase the breakdown voltage of a reverse biased semiconductor junction between said drift region and said body region.

2. The MOSFET of any one of claims 1, wherein said dielectric comprises a metal oxide insulator.

3. The MOSFET of claim 2, wherein said metal oxide insulator comprises a single or multi layer oxide insulator.

4. The MOSFET of any one of claims 1 to 3, wherein said dielectric is formed having a thickness t_{ox}, so that the

relationship $N_d \approx [(\varepsilon_{si} . E_0^2 . \varepsilon_{ox}^{4/3}) / (2 . q^{7/3})]^{3/7} . [t_{ox} . w]^{-4/7}$ is satisfied, where N_d is the concentration of dopant in said drift region, **2w** is a thickness of said drift region, ε_{ox} is the dielectric constant for said dielectric, ε_{si} is the dielectric constant for said drift region, E_0 is the electric field avalanche value for said drift region and q is the electron charge.

5. The MOSFET of claim 4, wherein a ratio of said width of said dielectric and a half width of said conducting region to a half width of said drift region is approximately 4:3.

6. The MOSFET of any one of claims 1 to 4, wherein said conducting region comprises a poly-silicon layer along an extent of said opposite one of said opposing sides of said dielectric.

7. The MOSFET of any one of claims 1 to 6, wherein said semiconductor wafer is formed of silicon.

8. The MOSFET of claim 7, wherein said semiconductor wafer is formed of n type silicon.

9. The MOSFET of any one of claims 1 to 8, wherein said conductive region comprises a polysilicon.

10. The MOSFET of any one of claims 1 to 9, further comprising another dielectric having opposing sides, one of its opposing sides extending alongside a second side of said drift region, and an opposite one of its opposing sides connected to a conducting region, so that a voltage across said dielectric between its opposing sides exerts an electric field into said drift region to redistribute free carriers in said drift region and thereby affect the electrical field distribution in said drift region to increase the breakdown voltage of a reverse biased

semiconductor junction between said drift region and said body region.

11. The MOSFET of any one of claims 1 to 10, further comprising an electrical contact, electrically connecting said source region and said conducting region.

12. The MOSFET of any one of claims 1 to 10, further comprising:

an electrical contact, electrically connected to said source region and isolated from said conducting region and said dielectric;

a second electrical contact electrically interconnected with said conducting region to allow application of a control voltage to control a voltage across said dielectric and thereby influence said breakdown voltage of said reverse biased semiconductor junction between said drift region and said body region.

13. A method of forming a metal oxide semiconductor transistor (MOSFET) in a semiconductor wafer comprising:

forming opposed vertically extending trenches in said semiconductor wafer;

covering interior walls of each of said trenches with a dielectric material of a defined thickness;

filling a volume of each of said trenches between said dielectric material with a conductive material;

forming a double diffused MOSFET structure between said opposed vertical trenches, said MOSFET structure formed to have a drift region that abuts said dielectric material along at least a portion of its vertical extent.

14. The method of claim **13**, wherein said defined thickness of said dielectric is t_{ox}, and t_{ox} is chosen so that the relationship $N_d \approx [(\varepsilon_{si} . E_0^2 . \varepsilon_{ox}^{4/3}) / (\mathbf{2} . q^{7/3})]^{3/7} . [t_{ox} . w]^{-4/7}$ is satisfied, where N_d is the concentration of dopant in said drift region, **2w** is a the distance between vertical extending trenches, ε_{ox} is the dielectric constant for said dielectric, ε_{si} is the dielectric constant for said drift region, E_0 is the electric field avalanche value for said drift region, and q is the electron charge.

15. The method of claim 13 or 14, wherein said covering is formed by wet oxidation.

16. The method of any one of claims 13 to 15, wherein said wafer is formed of silicon.

17. The method of any one of claims 13 to 16, wherein said conductive material comprises a polysilicon.

18. The method of claim 17, wherein said polysilicon comprises $POCl_3$ doped silicon.

19. The method of any one of claims 13 to 18, wherein each of said trenches are formed by forming and combining a plurality of proximate trenches thinner than said each of said opposed vertical trenches.

20. The method of any one of claims 13 to 19, wherein said double diffused MOSFET structure comprises a planar gate.

21. The method of any one of claims 13 to 19, wherein said double diffused MOSFET structure comprises a trenched gate.

22. The method of any one of claims 13 to 21, further comprising doping said region between said trenches with desired impurities using a tilted implantation process.

23. A n-channel or p-channel power metal oxide semiconductor field effect transistor (MOSFET), comprising:

a source region;

a drain region;

a gate;

a body region;

a drift region extending between said body region and drain region, to at least partially guide current from said source region to said drain region;

two dielectric columns each having opposing sides, one opposing side of each of said two dielectric columns extending alongside said drift region, and an opposite one of said opposing sides of each of said dielectric columns electrically connected to a conducting region, so that a voltage across each of said two dielectric columns between its opposing sides exerts an electric field into said drift region to redistribute free carriers in said drift region and thereby affect the electrical field distribution in said drift region to increase the breakdown voltage of a reverse biased semiconductor junction between said drift region and said body region.

24. The MOSFET of claim 23, wherein said drift region extends vertically between said source region and said drain region.

25. The MOSFET of claim 23, wherein said drift region extends laterally between said source region and said drain region.

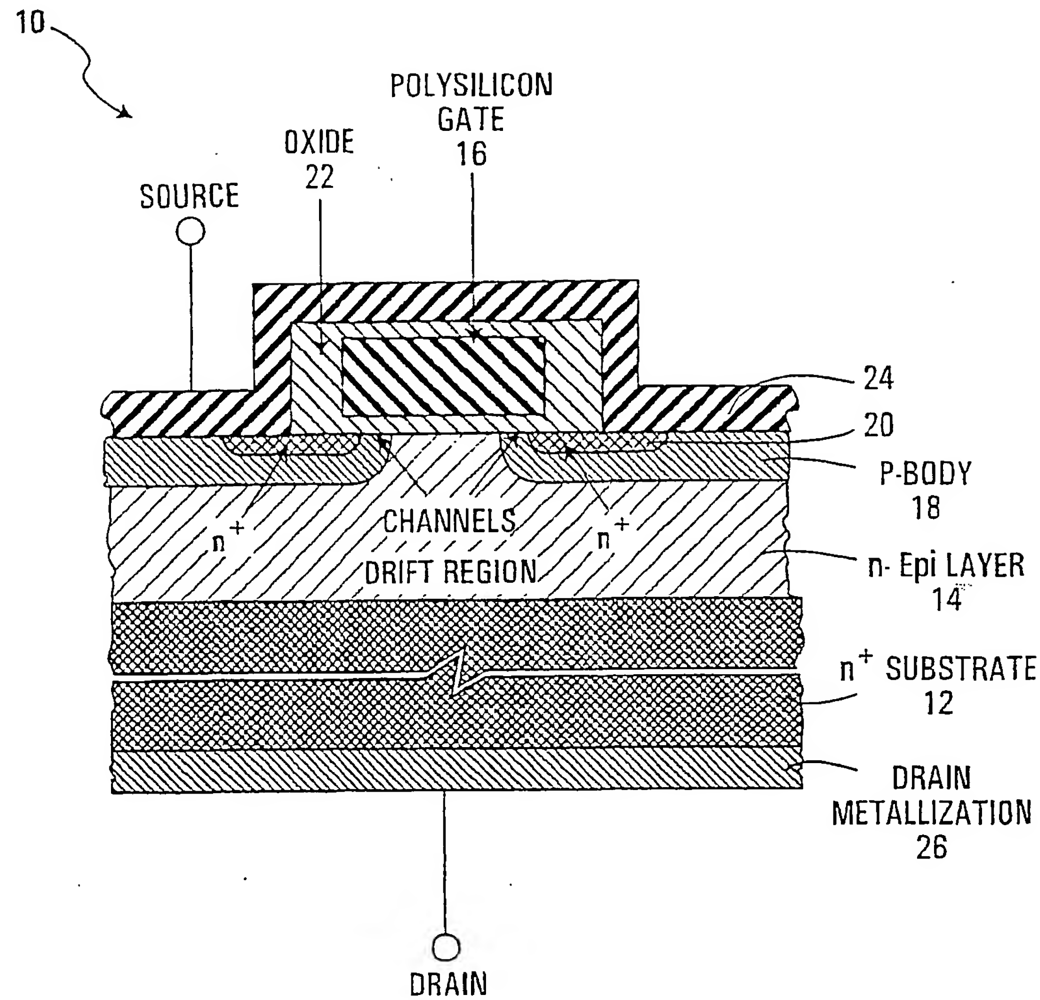

10
POLYSILICON
GATE
16
OXIDE
22
SOURCE
24
20
P-BODY
18
n+
CHANNELS
n+
DRIFT REGION
n- Epi LAYER
14
n+ SUBSTRATE
12
DRAIN
METALLIZATION
26
DRAIN

FIG. 1

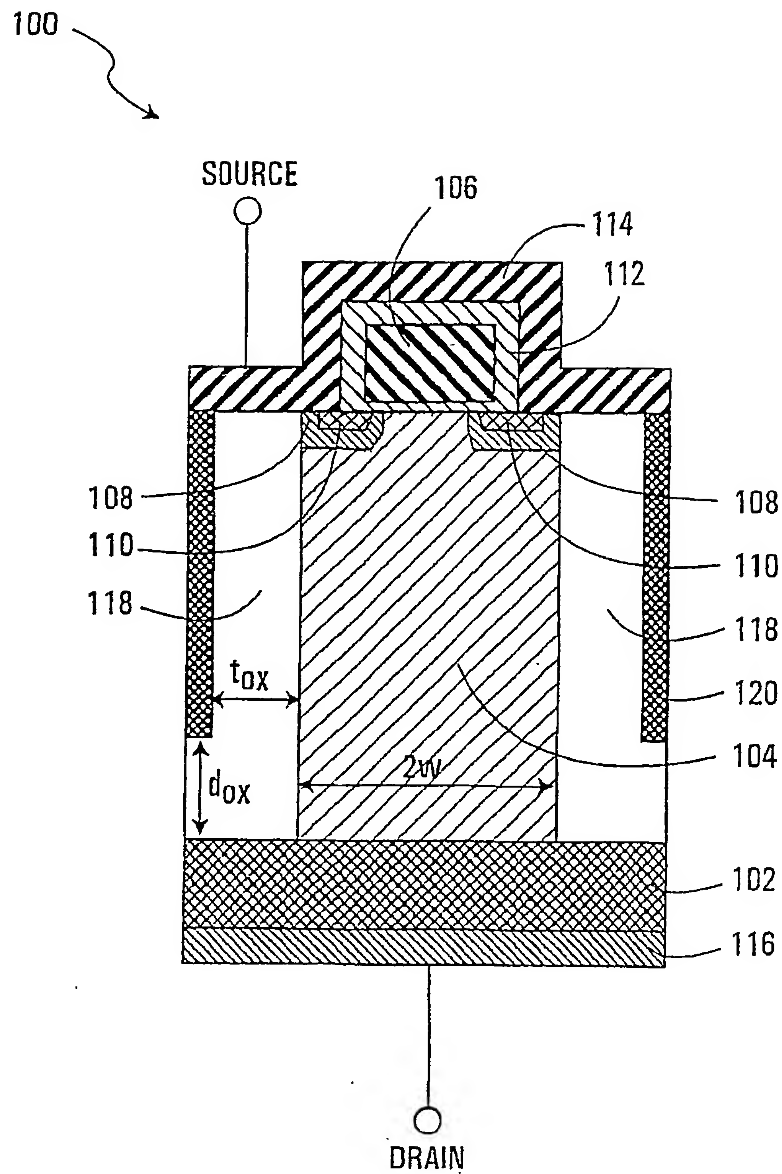

100
SOURCE
106
114
112
108
110
118
t_{ox}
d_{ox}
2w
108
110
118
120
104
102
116
DRAIN

FIG. 2A

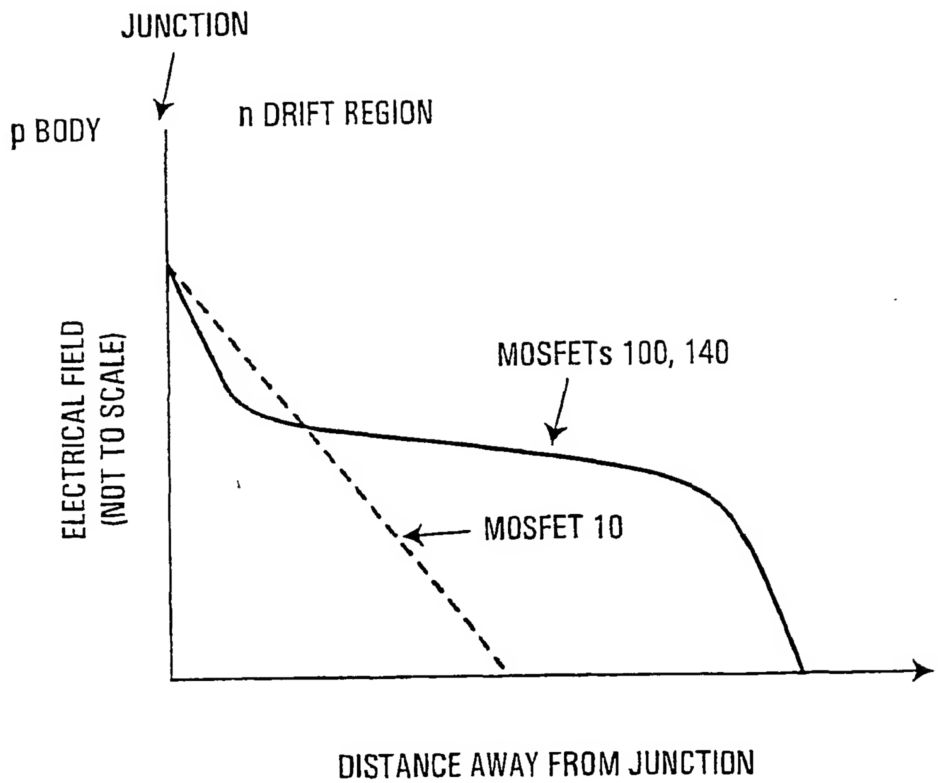

JUNCTION
p BODY
n DRIFT REGION
ELECTRICAL FIELD
(NOT TO SCALE)
MOSFETs 100, 140
MOSFET 10
DISTANCE AWAY FROM JUNCTION

FIG. 2B

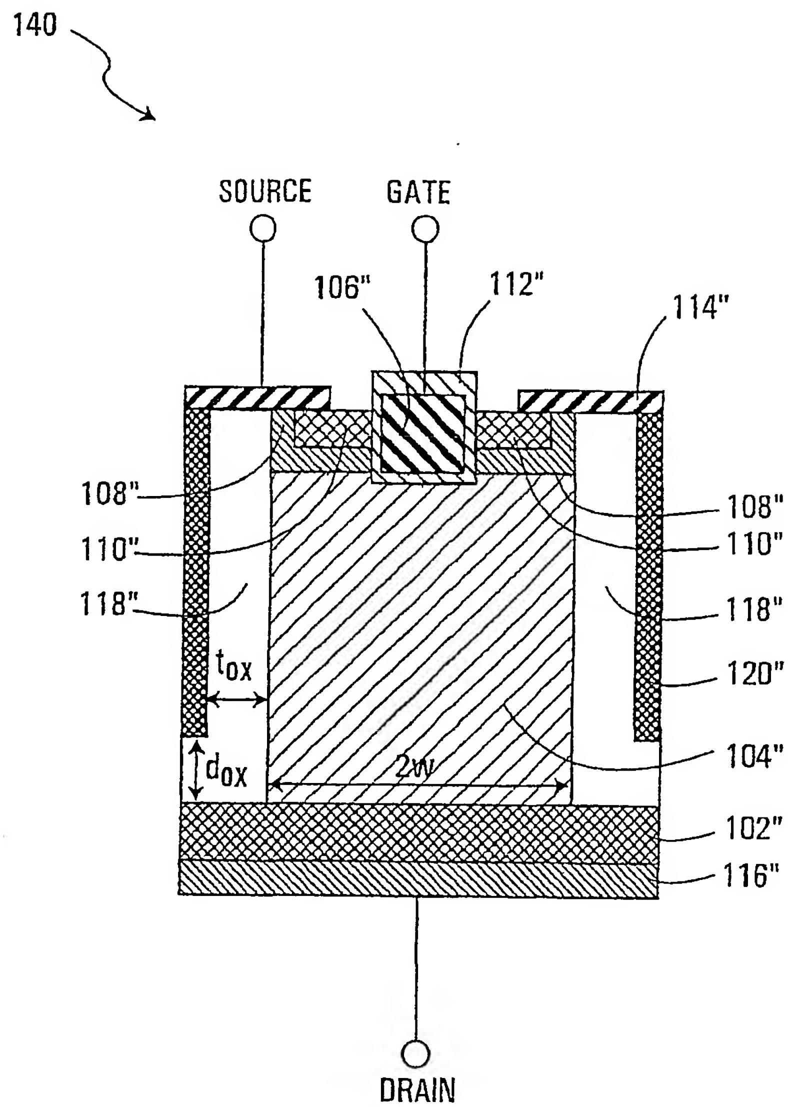

140
SOURCE
GATE
106"
112"
114"
108"
110"
118"
t_{ox}
d_{ox}
2w
108"
110"
118"
120"
104"
102"
116"
DRAIN

FIG. 3

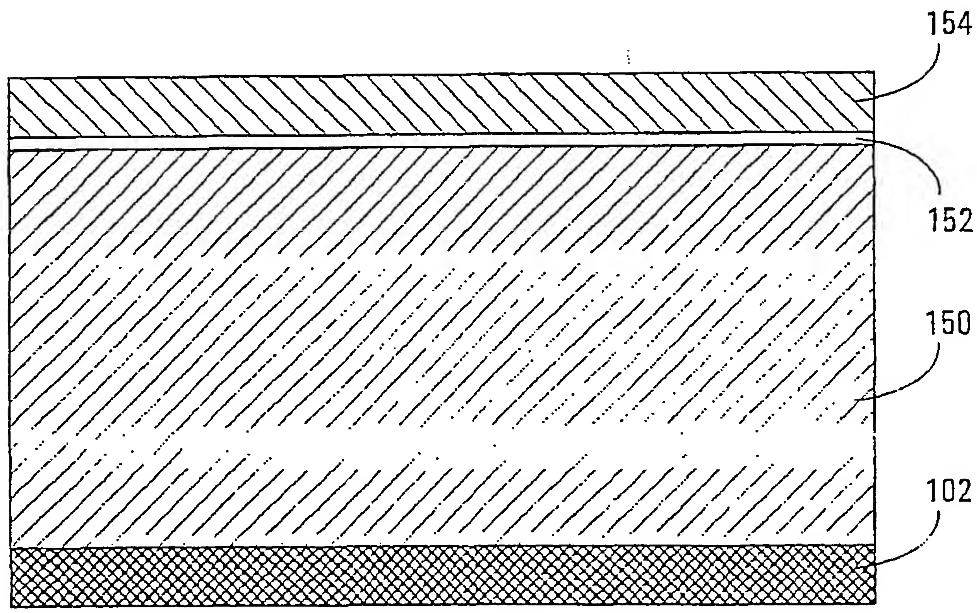


FIG. 4

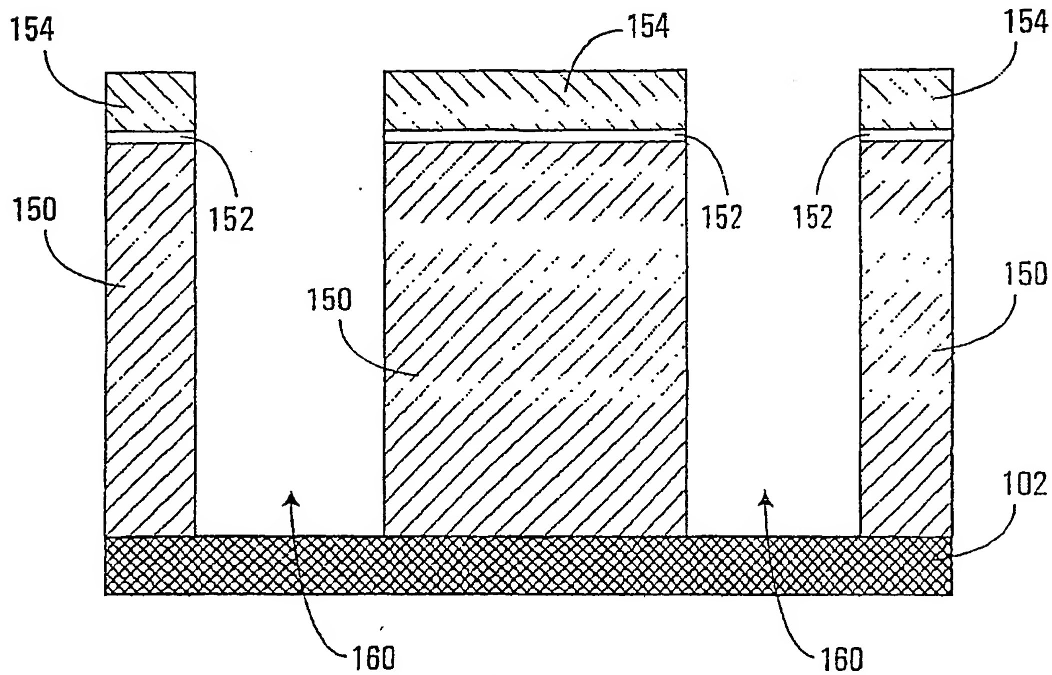

154
154
154
150
152
152
152
150
150
102
160
160

FIG. 5A

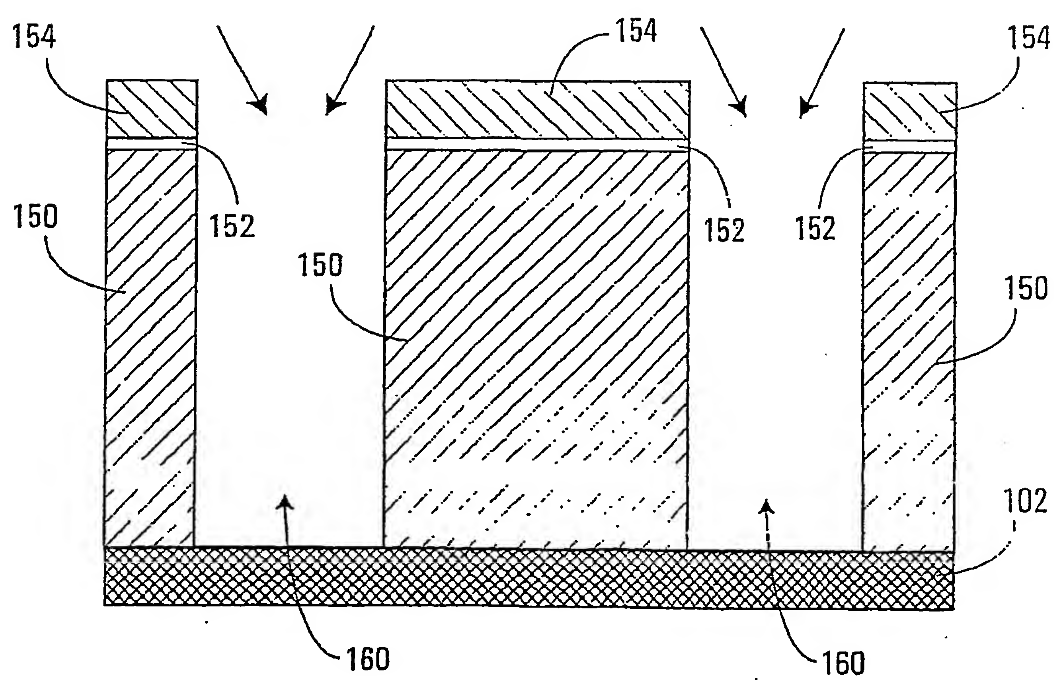

154
154
154
150
152
152
152
150
150
102
160
160

FIG. 5B

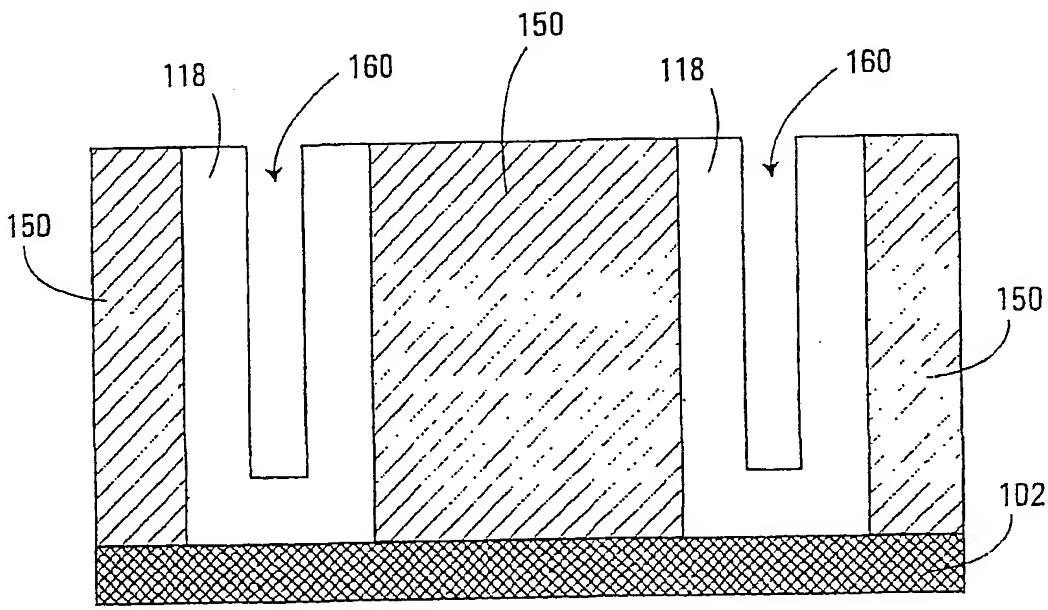


FIG. 6A

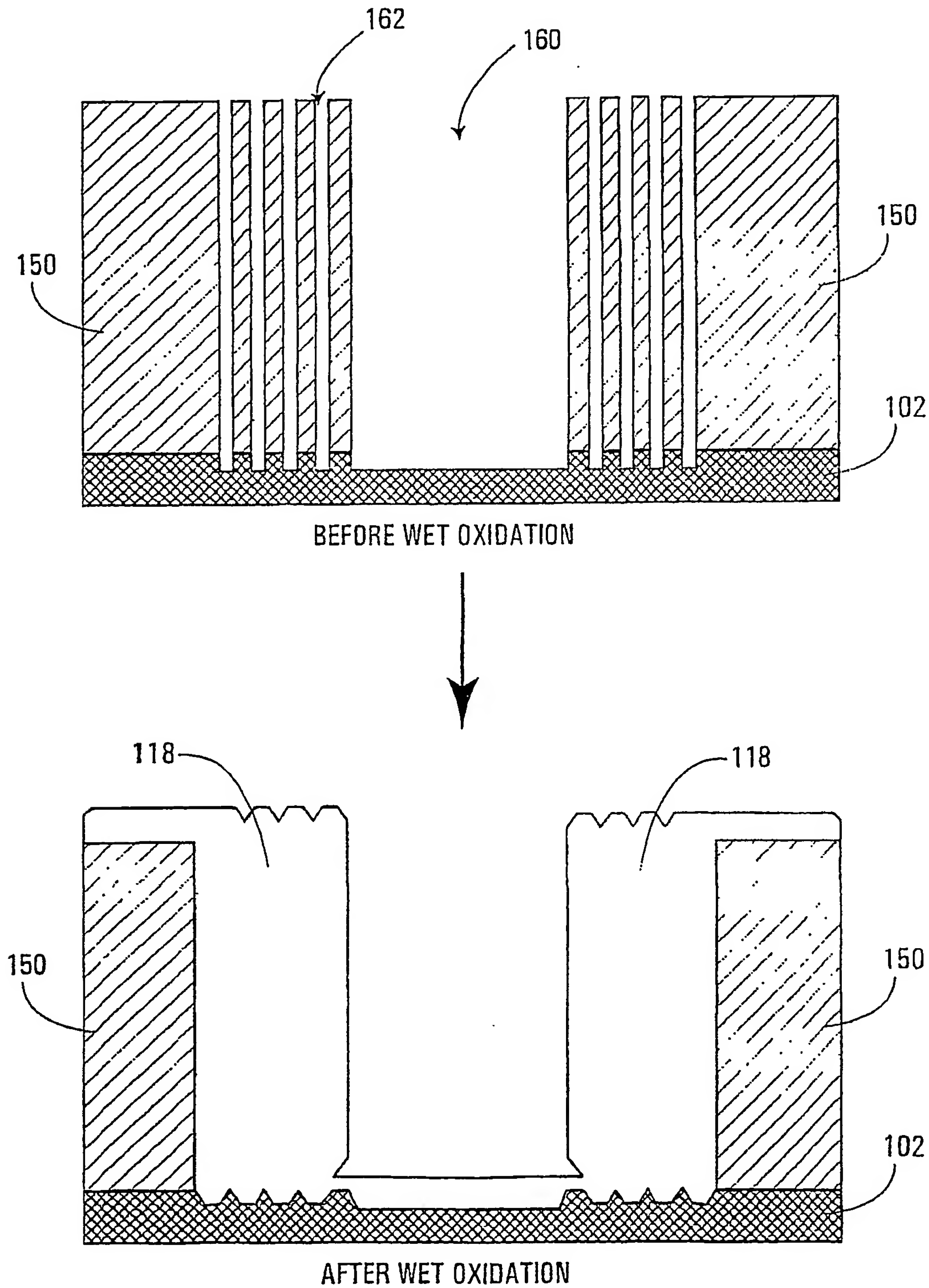

162
160
150
150
102
BEFORE WET OXIDATION
118
118
150
150
102
AFTER WET OXIDATION

FIG. 6B

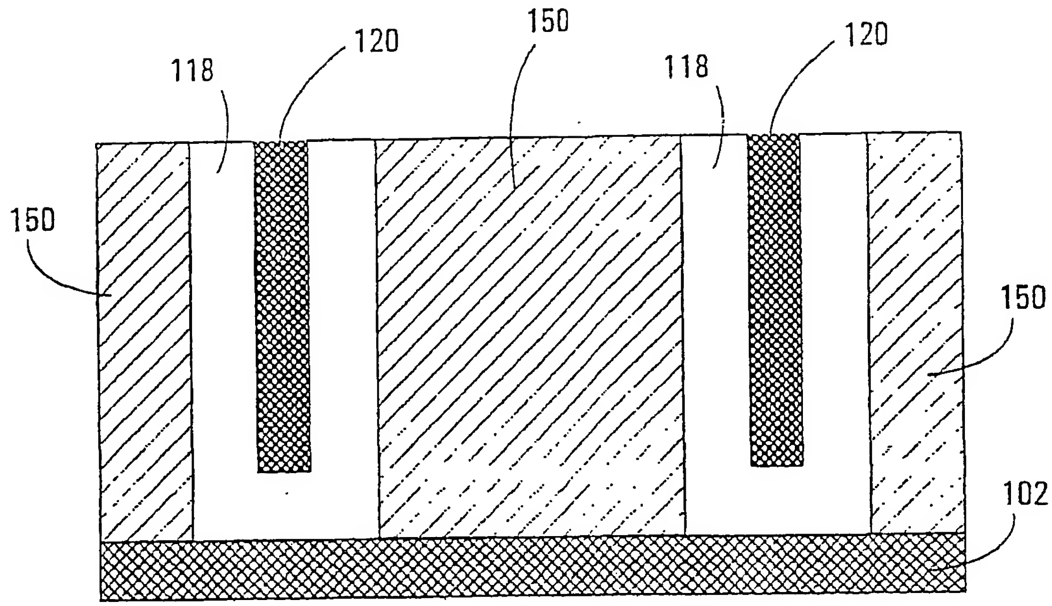


FIG. 7

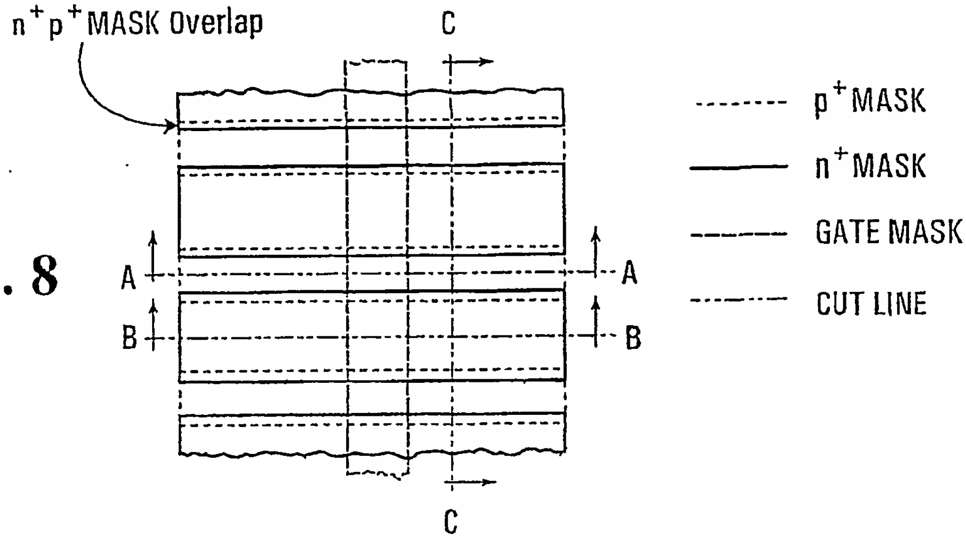


FIG. 8

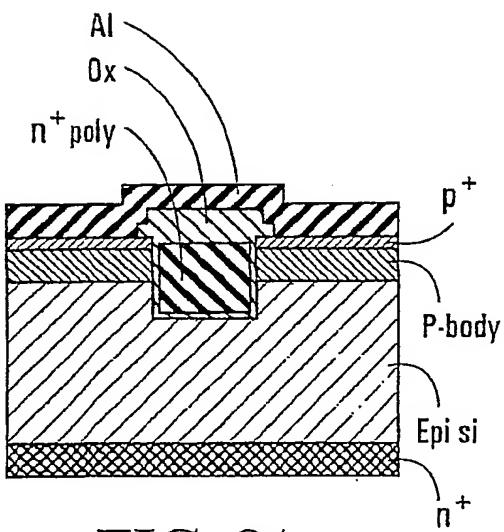


FIG. 8A

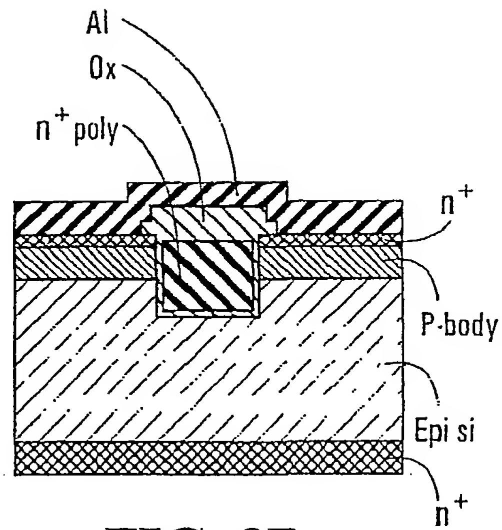


FIG. 8B

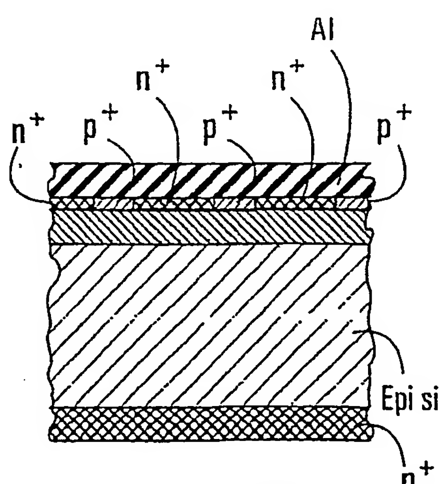


FIG. 8C

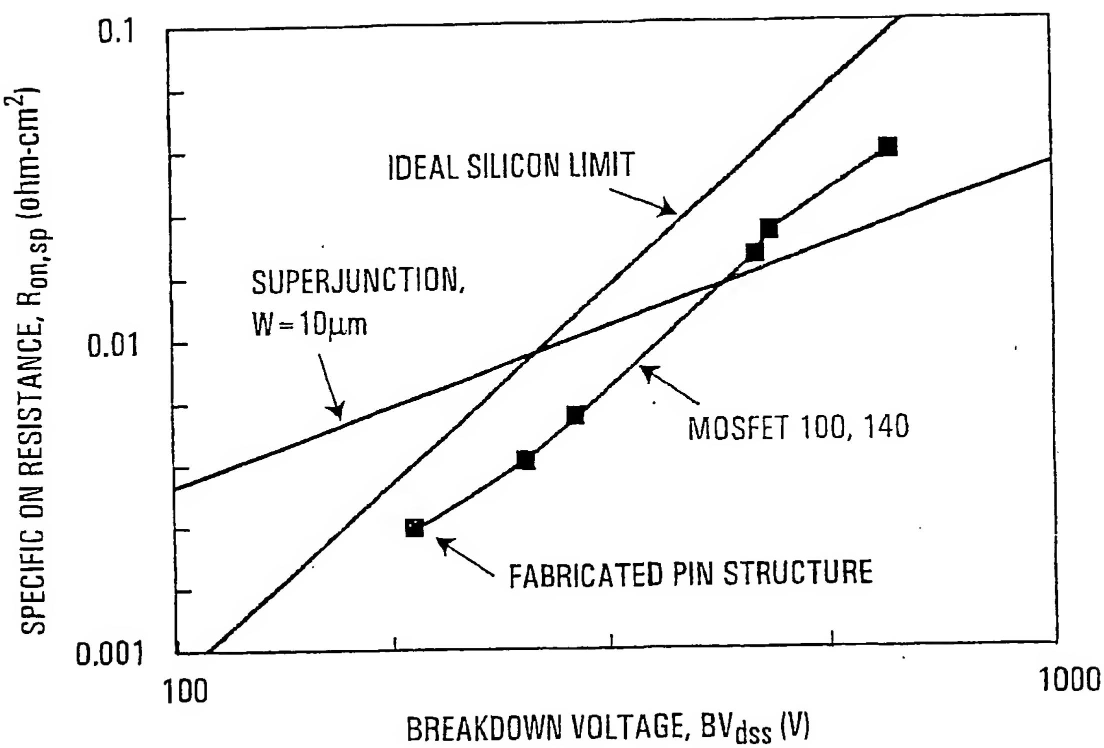

0.1
0.01
0.001
100
1000
SPECIFIC ON RESISTANCE, $R_{on,sp}$ (ohm-cm^2)
BREAKDOWN VOLTAGE, BV_{dss} (V)
IDEAL SILICON LIMIT
SUPERJUNCTION,
W=10μm
MOSFET 100, 140
FABRICATED PIN STRUCTURE

FIG. 9

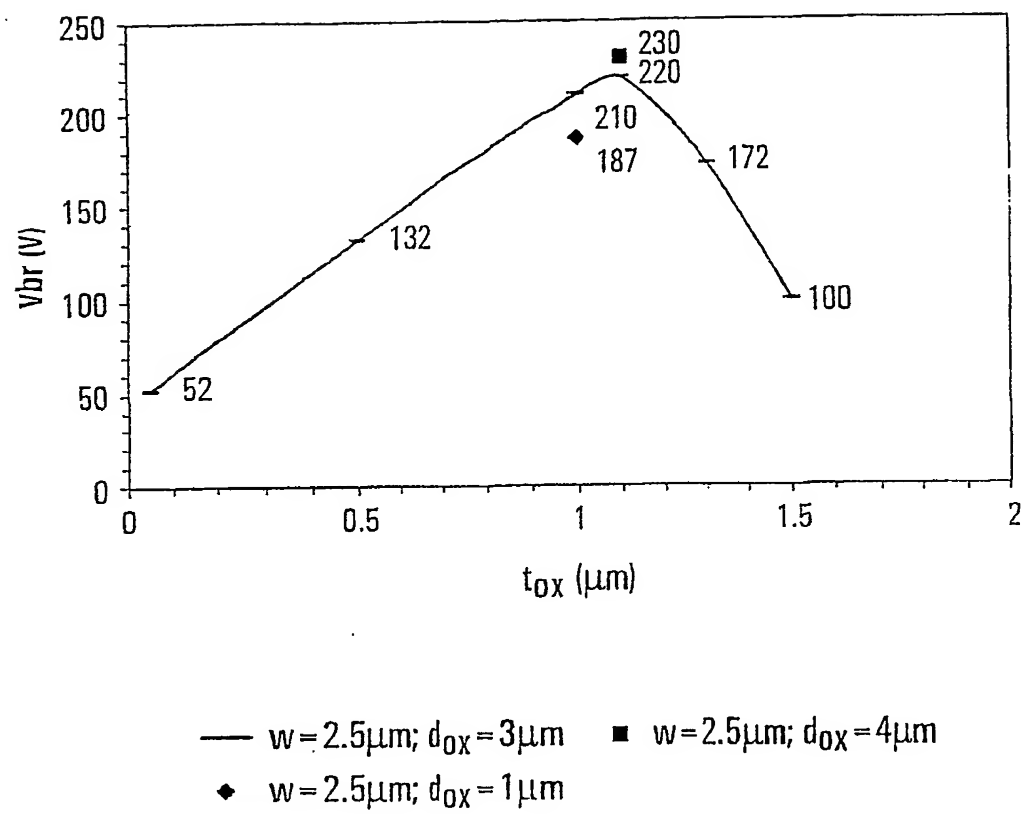

250
200
150
100
50
0
Vbr (V)
0
0.5
1
1.5
2
t_{ox} (µm)
230
220
210
187
172
132
100
52
w=2.5µm; d_{ox}=3µm
w=2.5µm; d_{ox}=4µm
w=2.5µm; d_{ox}=1µm

FIG. 10

MAG = 10000 kV = 1.4 WD = 13.0

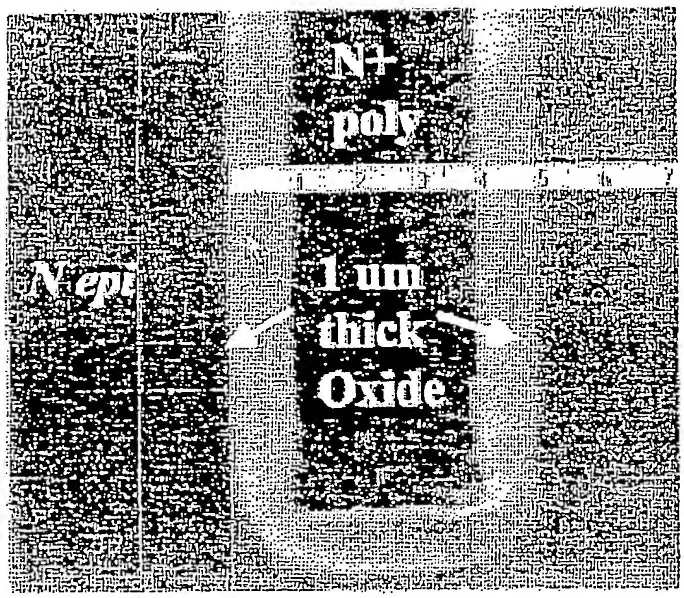


FIG. 11

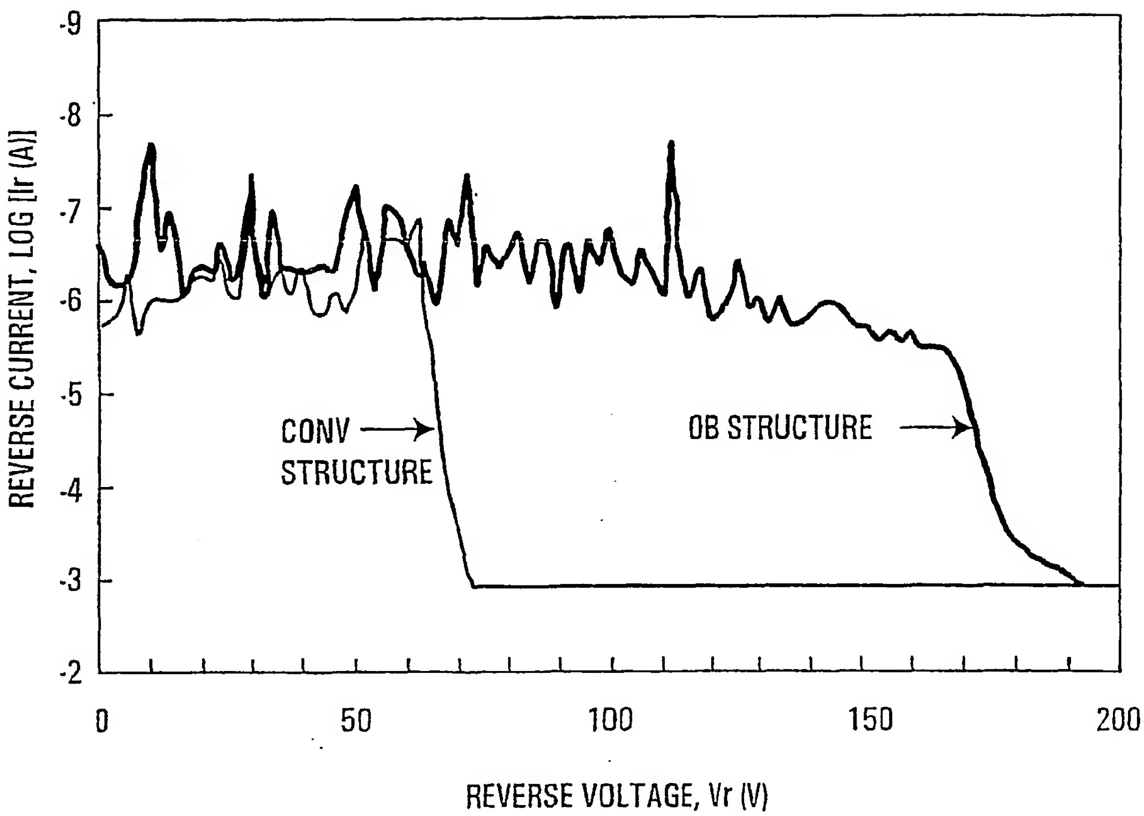

-9
-8
-7
-6
-5
-4
-3
-2
REVERSE CURRENT, LOG [Ir (A)]
CONV
STRUCTURE
OB STRUCTURE
0
50
100
150
200
REVERSE VOLTAGE, Vr (V)

FIG. 12

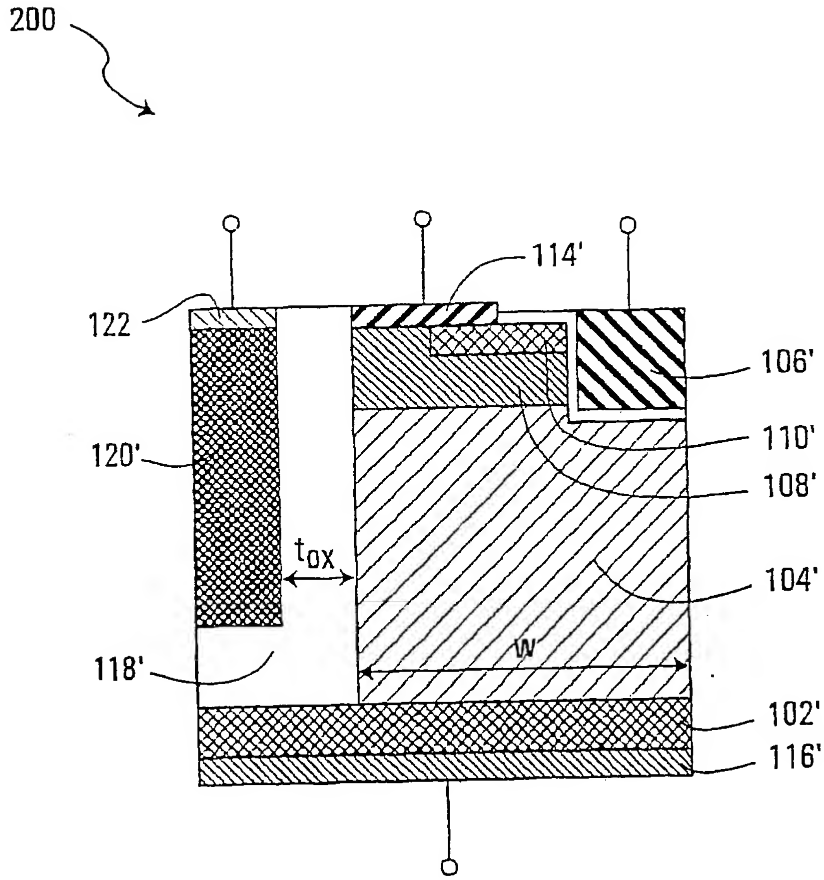


FIG. 13

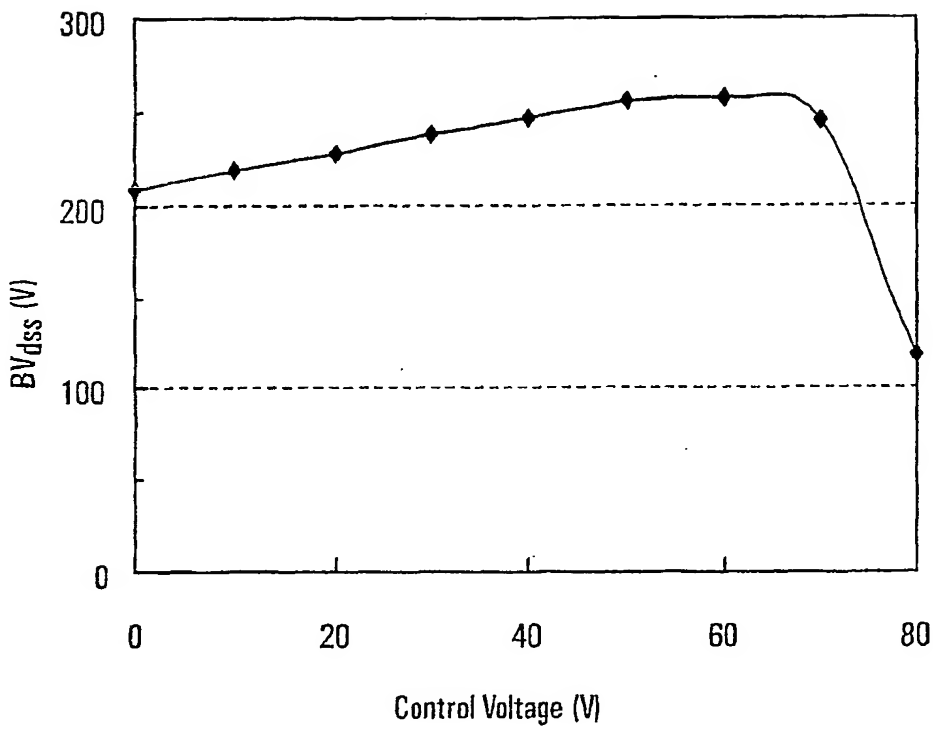
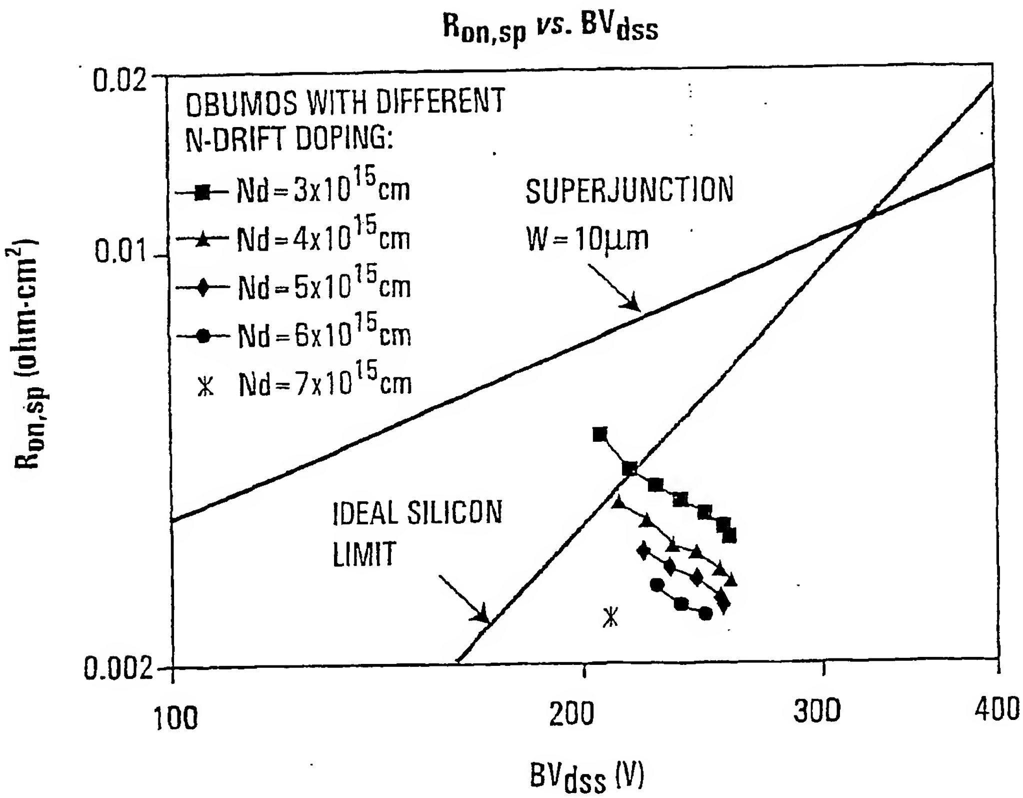
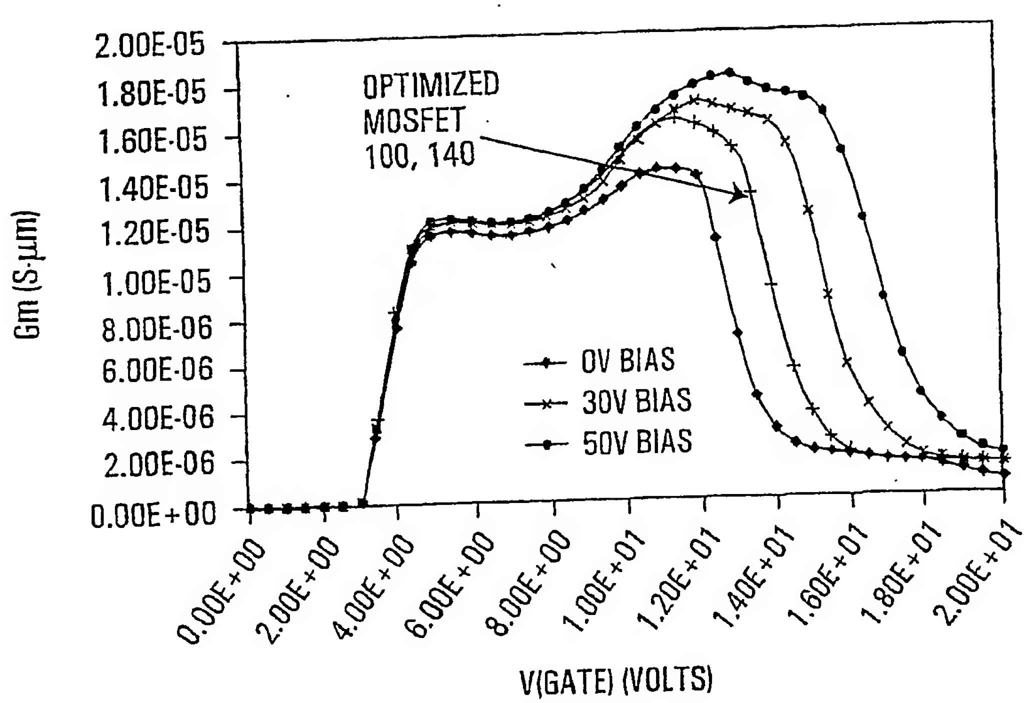


FIG. 14



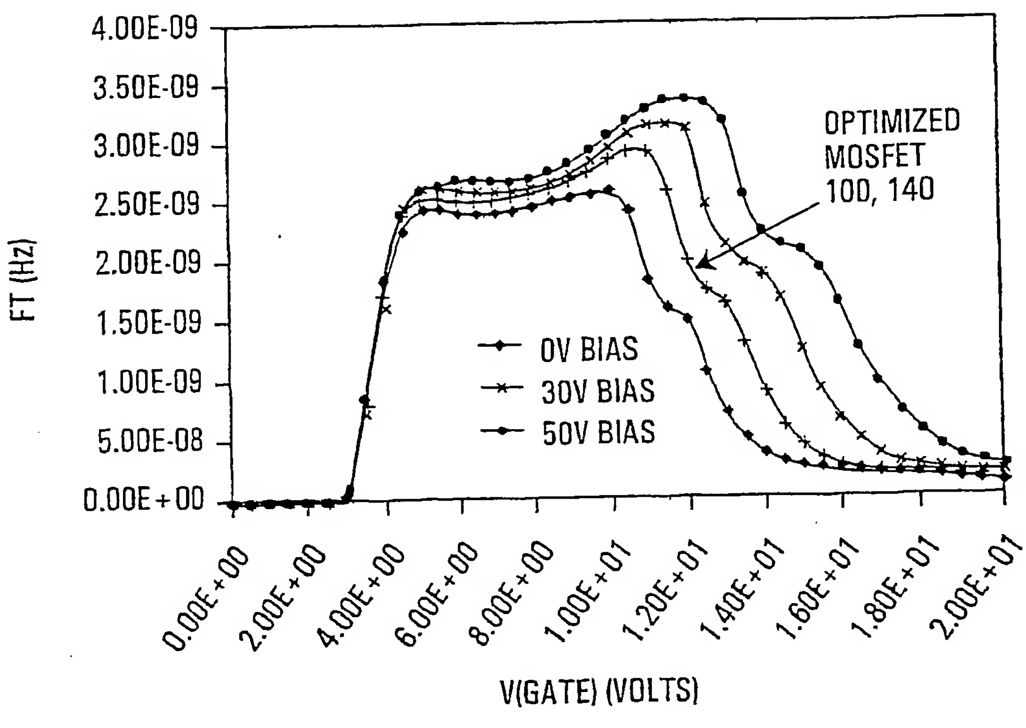
$R_{on,sp}$ *vs.* BV_{dss}
0.02
0.01
0.002
OBUMOS WITH DIFFERENT
N-DRIFT DOPING:
Nd=3x10^15cm
Nd=4x10^15cm
Nd=5x10^15cm
Nd=6x10^15cm
Nd=7x10^15cm
SUPERJUNCTION
W=10μm
IDEAL SILICON
LIMIT
$R_{on,sp}$ (ohm·cm²)
100
200
300
400
BV_{dss} (V)

FIG. 15



2.00E-05
1.80E-05
1.60E-05
1.40E-05
1.20E-05
1.00E-05
8.00E-06
6.00E-06
4.00E-06
2.00E-06
0.00E+00
Gm (S·µm)
OPTIMIZED
MOSFET
100, 140
0V BIAS
30V BIAS
50V BIAS
0.00E+00
2.00E+00
4.00E+00
6.00E+00
8.00E+00
1.00E+01
1.20E+01
1.40E+01
1.60E+01
1.80E+01
2.00E+01
V(GATE) (VOLTS)

FIG. 16



4.00E-09
3.50E-09
3.00E-09
2.50E-09
2.00E-09
1.50E-09
1.00E-09
5.00E-08
0.00E+00
FT (Hz)
OPTIMIZED MOSFET 100, 140
0V BIAS
30V BIAS
50V BIAS
0.00E+00
2.00E+00
4.00E+00
6.00E+00
8.00E+00
1.00E+01
1.20E+01
1.40E+01
1.60E+01
1.80E+01
2.00E+01
V(GATE) (VOLTS)

FIG. 17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG02/00113

A.	**CLASSIFICATION OF SUBJECT MATTER**
Int. Cl. [7]:	H01L 029/78, 21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B.	**FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DWPI, JAPIO; (H01L 29/78, 21/336, H01L and MOSFET), drift, (power, high current, double diffused), (trench, groove), (breakdown, high voltage), (dielectric, oxide, insulator)

C.	**DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 00/68997 A1 (C.P. CLARE CORPORATION) 16 November 2000 See the abstract, fig 8, page 12 line 21-30	1-25
X	JP 2000-349288 A (FUJI ELECTRIC CO LTD) 15 December 2000 Figures and translation from www1.ipdl.jpo.go.jp/PA1/cgi-bin/PA1INDEX	1-25
P,A	WO 01/95398 A1 (GENERAL SEMICONDUCTOR, INC) 13 December 2001 See the Abstract	

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 July 2002	29 JUL 2002

Name and mailing address of the ISA/AU	Authorized officer
AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	I.A.BARRETT Telephone No : (02) 6283 2189

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 00/74146 A1 (MICRO-OHM CORPORATION) 7 December 2000 See the abstract	
P,A	Patent Abstracts of Japan, JP 2001-267570 A (MITSUBISHI ELECTRIC CORP) 28 September 2001 See the abstract	
A	Patent Abstracts of Japan, JP 2001-111050 A (TOYOTA CENTRAL RES & DEV LAB INC) 20 April 2001 See the abstract	
A	Patent Abstracts of Japan, JP 11-017176 A (HITACHI LTD) 22 January 1999 See the abstract	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/SG02/00113

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
WO	200068997	AU	200048201				
JP	2000349288	NONE					
WO	200195398	AU	200054584	AU	200175105	AU	200175189
		EP	1192640	WO	200075965	WO	200195385
		US	2002009832	US	2002014658	US	2002066924
WO	200074146	AU	200051730	EP	1198843	US	6191447
		US	2001000033				
JP	2001267570	NONE					
JP	2001111050	NONE					
JP	11017176	NONE					

END OF ANNEX